IN THE SPECIFICATION:

Please amend paragraph number **[0002]** as follows:

[0002] The present invention relates generally ~~relates~~ to integrated circuit design and fabrication. Specifically, the present invention relates to semiconductor fuses, methods for fabricating the semiconductor fuses, methods for using the semiconductor fuses, and semiconductor devices containing the semiconductor fuses.

Please amend paragraph number **[0004]** as follows:

[0004] Another type of memory device is a programmable read only memory (PROM) device. Unlike ROM devices, PROM devices are programmable after their design and fabrication. To render them programmable, PROM devices are typically provided with an electrical connection in the form of a fusible link (fuse). There are a considerable number of fuse designs used in PROM devices, such as those disclosed in IEEE Transactions on Electron Devices, Vol. 33, No. 2, p. 250-253 (Feb. 1986), and in U.S. Patent Nos. 5,589,706, 4,491,860, 5,625,218, 4,796,075, and 4,740,485, the disclosures of each of which are incorporated herein by reference. Perhaps the most common fuse design is a metal or polysilicon layer which is narrowed or "necked down" in one region. To blow the fuse, a relatively high electrical current is driven though the metal or polysilicon layer. The current heats the metal or polysilicon above its melting point, thereby breaking the conductive link and making the metal layer or polysilicon discontinuous. Usually, the conductive link breaks in the narrowed region because the current density (and temperature) is highest in that region. The PROM device is thus programmed to conducting and non-conducting patterns, thereby forming the 1 or 0 comprising the data stored in the memory device.

Please amend paragraph number **[0005]** as follows:

[0005] Rather than employing an electrical current, a laser can be employed to blow the fuses. Using lasers instead of electrical current to blow fuses, however, has become more difficult as the size of memory devices decreases. As memory devices decrease in size and the degree of integration increases, the critical dimensions (e.g., fuse pitch) of memory cells become

smaller. The availability of lasers suitable to blow the fuse becomes limited since the diameter of the laser beam should not be smaller than the fuse pitch. Thus, the fuse pitch, and the size of memory devices, becomes dictated ~~by~~ by the minimum diameter of laser beams obtainable by current laser technology.

Please amend paragraph number **[0006]** as follows:

[0006] The ability of electrical currents to blow fuses could aid in adapting fuses for a variety of applications, such as redundancy technology. Redundancy technology improves the fabrication yield of high-density memory devices, such as SRAM and DRAM devices, by replacing failed memory cells with spare ones using redundant ~~circuitry~~ circuitry, which is activated by blowing fuses. Using laser beams to blow the fuses limits the size and, therefore, the number of memory devices as explained above since the diameter of a conventional laser beam is about 5 microns. Using electrical currents instead to blow fuses, therefore, has a greater potential for high-degree integration and decreased size of memory devices.

Please amend paragraph number **[0007]** as follows:

[0007] The present invention generally provides fuses for integrated circuits and semiconductor devices, methods for making the same, methods of using the same, and semiconductor devices containing the same. The semiconductor fuse of the present invention contains two conductive ~~layers an~~ layers — overlying layer and an underlying ~~layer disposed~~ layer — disposed on an insulating substrate. The underlying layer comprises a refractory metal nitride, such as titanium nitride, and the overlying layer comprises tungsten silicide. The semiconductor fuse may be fabricated during manufacture of local interconnect structures containing the same materials.

Please amend paragraph number **[0012]** as follows:

[0012] The ~~Figures~~ figures presented in conjunction with this description are not actual views of any particular portion of an actual semiconductor device or component, but are merely representations employed to more clearly and fully depict the present invention. Figures 1-5

and 7 are cross-sectional ~~side views~~ side views of steps of one exemplary process for making fuses according to the present invention, and the resulting fuse. Figure 6 is a cross-sectional top view of a fuse element according to the present invention.

Please amend paragraph number **[0015]** as follows:

[0015] Figures 1-7 illustrate the steps of one exemplary method for forming a semiconductor fuse according to the present invention and the resulting structures. As illustrated, the inventive semiconductor fuse can be formed simultaneously ~~with~~ with, and integrated ~~with~~ with, the process of forming an IC device containing a local ~~connect~~ interconnect (LI) structure. It will be understood, however, by those skilled in the art that other semiconductor fuses and/or ICs could be formed by slight modifications of the illustrated method.

Please amend paragraph number **[0019]** as follows:

[0019] Next, as shown in Figure 2, silicon nitride layer 8 and pad oxide layer 4 are patterned by any suitable process known in the art, thereby removing undesired portions of silicon nitride layer 8 and pad oxide layer 4 above portions of substrate 2 where field isolation regions 10 will be formed and leaving silicon nitride layer 8a and pad oxide layer 4a. The structure in Figure 2 is illustrated in two ~~portions portion~~ portions — portion 200 containing the to-be-formed fuse and portion 100 containing the to-be-formed local interconnect ~~structure separated~~ structure — separated by the vertical dotted line. Any suitable patterning process known in the art, such as a photolithographic pattern and etch process, can be used to pattern silicon nitride layer 8 and pad oxide layer 4. For example, a photoresist film can be spun on silicon nitride layer 8, developed, and portions thereof removed to leave photoresist mask 9 (shown by the dotted line in Figure 1). Using photoresist mask 9, the undesired portions of silicon nitride layer 8 and pad oxide layer 4 are then removed by any suitable anisotropic etching process to obtain silicon nitride layer 8a and pad oxide layer 4a. Photoresist mask 9 may then be removed by any suitable process known in the art which does not attack silicon nitride layer 8a or substrate 2.

Please amend paragraph number **[0020]** as follows:

[0020] Next, as depicted in Figure 2, at least one isolation region (illustratively represented as isolation region 10) is formed in substrate 2 by any suitable process known in the art. For example, field isolation region 10 may be formed by any suitable process employing silicon nitride layer 8a as a mask, such as a trench-and-refill or local oxidation of silicon (LOCOS) process. Preferably, as illustrated in Figure 2, isolation regions 10 are field oxide regions formed by a LOCOS process, which oxidizes the surface of preferred silicon substrate 2 in areas where silicon nitride layer 8 and pad oxide layer 4 have been removed to form recessed oxide regions due to the consumption of silicon. The thickness of isolation regions 10 may range from about 2000 to about 4000 angstroms. After forming isolation regions 10, silicon nitride layer 8a and pad oxide layer 4a are removed to expose substrate 2 by any suitable process known in the art which does not attack substrate 2 and minimizes attack of field isolation regions 10. Preferably, when isolation ~~regions~~ regions 10 comprise silicon oxide, silicon nitride layer 8a and pad oxide layer 4a are removed by a wet etch process using phosphoric acid and/or hydrofluoric acid.

Please amend paragraph number **[0021]** as follows:

[0021] Next, as depicted in Figure 3, dielectric layer 12 is formed over substrate 2 and optionally over isolation regions 10. Any dielectric material suitable as a gate dielectric, such as doped or undoped silicon oxide, organic dielectric materials, boron and/or phosphorous doped silicate glass, silicon oxynitride, or silicon nitride, or a composite layer of these materials, can be used as dielectric layer 12. Preferably, dielectric layer 12 is a silicon oxide layer formed by thermally oxidizing the preferred silicon substrate 2 to form a high-quality silicon oxide layer with little to no contamination. The preferred silicon oxide layer is formed primarily over the exposed regions of substrate 2, but may be formed over isolation regions 10 if the silicon oxide layer is deposited rather than thermally grown. The thickness of dielectric layer 12 may range from about 50 to about 150 angstroms.

Please amend paragraph number **[0022]** as follows:

[0022] Next, polysilicon layer 14 is formed over dielectric layer 12 and field isolation regions 10. Polysilicon layer 14 may be formed by any suitable deposition method known in the art, such as physical or chemical vapor deposition. Preferably, polysilicon layer 14 is deposited by low-pressure CVD to a thickness ranging from about 800 to about 2000 angstroms. Polysilicon layer 14 is then doped, preferably with an n-type ~~dopant~~ dopant, such as phosphorous, by any suitable ion implantation or doping process known in the art. Alternatively, polysilicon layer 14 can be *in-situ* doped during deposition of polysilicon layer 14 by including a gas containing the desired dopant in the deposition atmosphere.

Please amend paragraph number **[0027]** as follows:

[0027] The Ti layer is then converted to a layer comprising titanium and nitrogen, such as Ti_xN_y where x can range from more than 0 to less than 1.0 ~~(hereafter~~ (hereafter "titanium nitride (or TiN) layer ~~24").~~ 24"). In one embodiment, this conversion is performed by annealing the Ti layer in a nitrogen-containing atmosphere for a time and temperature sufficient to convert the titanium to a mixture of titanium and nitrogen. In this annealing process, the temperature may range from about 600 to about 750°C., and is preferably about 650°C., and the time may range from about 20 to about 120 seconds, and is preferably about 60 seconds. The nitrogen-containing atmosphere of the annealing process may comprise a gas or a mixture of gases containing nitrogen, such as nitrogen, ammonia, or mixtures thereof. The annealing atmosphere may also contain other gases, such as argon or hydrogen. Preferably, the nitrogen-containing atmosphere contains substantially pure nitrogen gas.

Please amend paragraph number **[0030]** as follows:

[0030] Next, conductive layer 26 is patterned in the desired fuse pattern. This patterning can be performed by any suitable process known in the art, such as a photolithographic pattern and etch process. For example, a photoresist film can be spun on conductive layer 26, developed, and portions thereof removed to leave photoresist mask 23 (shown by the dotted line

in Figure 5). Using photoresist mask 23, portions of conductive layer 26 not underlying photoresist mask 23 are removed by any suitable anisotropic etching process known in the art.

Please amend paragraph number **[0032]** as follows:

[0032] This process of patterning conductive layer 26 and TiN layer 24 should be performed to obtain the desired LI structure 36 and to obtain the desired structure of fuse 34. One preferred structure ~~for~~ of an LI structure 36 is illustrated in Figure 7, where ~~local interconnect~~ an LI structure 36 has been fabricated to overlie gate structure 20 overlying isolation region 10. One preferred structure for fuse 34 is illustrated in Figures 6 and 7, where the fuse structure is disposed over isolation region 10 and contains at least two distinct regions: terminal portions or regions 28 and neck region or portion 30. Terminal regions 28 are patterned to accommodate metal contacts that will later be formed thereon. Thus, the size and shape of terminal regions 28 will vary depending on the number and types of metal contacts to be formed thereon. The pattern (e.g., length and width) of neck portion 30 depends on the desired fuse properties. Preferably, the length of neck portion 30 may range from about 1 to about 20 microns, and more preferably is about 3.5 microns. Preferably, the width of neck portion 30 may range from about 0.2 to about 1 micron, and more preferably is about 0.35 microns.

Please amend paragraph number **[0033]** as follows:

[0033] Neck portion 30 is that portion of fuse 34 that will blow when subjected to programming or sufficient electrical current. For the preferred dimensions of neck portion 30 above, when a sufficient amount of ~~current about~~ current — about 1 to about 25 mA and preferably about ~~5.5 mA flows~~ 5.5 mA — flows through conductive layer 26, it heats up and melts in neck portion 30, thereby interrupting the current flow. Neck portion 30 blows before terminal portions 28 because, while the same amount of current runs through both, there is less area in neck portion 30. Consequently, the temperature of neck portion 30 is higher than the temperature in terminal portions 28, leading to quicker melting of conductive layer 26 in this region. Reducing the width-to-length ratio of neck portion 30 and changing the material of conductive layer 26 will change the amount of current needed to blow the ~~fuse.~~ fuse 34.

Tungsten silicide is the preferred material for conductive layer 26 since, when practiced in the present invention, the tungsten silicide requires only about half the electrical current to blow as a polysilicon fuse with similar dimensions. After the fuse is blown by this electrical current, the leakage current of the blown fuse ranges from about 1 to about 10 nA and is preferably less than about 1 nA.

Please amend paragraph number **[0036]** as follows:

[0036] Having thus described in detail the preferred embodiments of the present invention, it is to be understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above ~~description~~ description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.